

**In the Specification:**

Please amend paragraph [0007] as follows:

[0007] Various embodiments of methods and systems for implementing a microprocessor that fetches a group of instructions into instruction cache in response to a corresponding trace being evicted from the trace cache are disclosed. In some embodiments, a microprocessor may include an instruction cache, a trace cache, and a prefetch unit. In response to a trace being evicted from the trace cache, the prefetch unit may fetch a line of instructions into the instruction cache.